Europäisches Patentamt	Eur pean Patent Office	Office européen des brevets

Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00123770.0

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

DEN HAAG, DEN
THE HAGUE, 15/05/01
LA HAYE, LE

Europäisches Patentamt | European Patent Office | Office européen des brevets

Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.: 00123770.0
Demande n°:

Anmeldetag:
Date of filing: 01/11/00
Date de dépôt:

Anmelder:
Applicant(s):
Demandeur(s):
International Business Machines Corporation
Armonk, NY 10504
UNITED STATES OF AMERICA

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Selftest for leakage for driver/ receiver stages

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
/

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

D E S C R I P T I O N

Selftest for Leakage For Driver/ Receiver Stages

1. BACKGROUND OF THE INVENTION

1.1 FIELD OF THE INVENTION

The present invention realates to method and system for providing a test for leakage for driver/ receiver stages, and in particular for bi-directional input/ output stages of a semiconductor chip.

1.2 DESCRIPTION AND DISADVANTAGES OF PRIOR ART

Although the present invention has a very broad scope implied by its inherent technical abstractness it will be discussed in here primarily with reference to bidirectional chip input/ output (I/O) stages, because this is the most obvious technical area to apply the present invention and to draw enormous technical and economical advantages immediately from it.

The testing of semi-conductor chips in general is a very complex task because test devices must be fine enough in order to be coupled to the enourmous number of chip signal input-/ output pins which are available to test the chip with a given test schema.

The current and even more next generation semiconductor product chips have an increasingly huge amount of signal I/O stages to achieve the performance and complexity requirements imposed by the specific technical progress intended with each new generation. This trend, in conjunction with the required high quality of the products, results in the need for very cost

intensive test equipment to reach all of said signal input / output stages at the tester to get them adequately tested.

Adequate testing includes to test for input/ output leakage for driver/ receiver stages of an I/O stage.

The above mentioned test equipment required for said adequate testing comprises large and expansive apparatuses. In particular, the coupling between test apparatus and chip is difficult because of the enormous number of I/O stages to be tested. Nearly each new chip generation requires a new expensive test apparatus in particular to test the quality of said I/O stages.

In order to simplify chip testing in general, and in particular the testing of the driver and receiver capability a method was introduced, the so-called "reduced pin test method". The basic idea used in this prior art approach is to couple an intermediate, connective device having a reduced number of pins between the test apparatus and the chip to be tested. The testing scheme was then a 'structurized scheme', i.e., a scheme in which a selectively chosen subset of chip signal I/Os connected to the low pin count test apparatus and a specific set of test patterns, applied just via this test I/O interface was decided to be sufficient to test the respective chip and in particular by having the not-connected signal I/Os testing themselves by receiving their own driven value.

A prior art I/O stage is illustrated next below with reference to fig. 1 in order to show the prior art situation and the problems concerned with it:

Fig. 1 shows a simplified scheme of a prior art bidirectional signal I/O stage 10 having a built-in 'digital' selftest feature by which minimum qualitative properties of the driver 18 / receiver 24 system can be tested by driving both values '0' and '1' to the node 14, - generally a connective pad denoted as PAD in the figures - and by receiving it correspondingly in the

receiver 24 and the signal line 26 RDATA.

This kind of selftest, however, is of limited coverage only because it does not tell anything about the 'analogue', i.e., the electrical properties of the I/O stage, and in particular nothing about the leakage current between the off-chip connective node 14 and the supply voltage VDD, or ground, or any other voltage potential, potentially relevant, respectively.

Said I/O stage 10 further comprises a signal line 12 DDATA as a signal input representing the logical data value ('0' or '1') which has to be driven out by the driver logic 18 to the node 14 denoted as PAD as the off-chip connection thereof. The signal line 16 carries a signal denoted as ACT which is the signal input used for ACTivating and turning off the driver when the signal I/O stage 10 has to be in receive mode. The P-type 20 and N-type 22 output stage field effect transistors, referred to herein and denoted in the drawing as P and N (FETs) are connected to the node 14 PAD.

The P and N transistor devices depicted in fig. 1 are illustrated in a simplified way only, in order to improve clarity. In reality each device 20 and 22 comprises a plurality single transistors, which is in turn often called 'signal driver'.

The receiver device 24 denoted as 'rec' converts the voltage levels applied at node 14 PAD to logical '0' and '1' values at the signal line 26 denoted as RDATA often further connected to a Master/ Slave latch. Having implemented said limited selftest capability the signal I/O stage 10 receives its own driven output signal.

In this situation where the signal I/O stage receives its own driven output signal by having the driver in low impedance mode, a potential defect causing leakage paths or erronous driver high

impedance, i.e., OFF state behavior may not be detected explicitly.

In particular, the off-chip connection PAD is not fully tested for leakage paths to VDD, GND or any other potential, nor can a defect, causing a low impedance at the P or N device be detected when it should be in high-impedance mode, abbreviated herein as HZ-mode. Whenever the signal I/O stage is in HZ-mode, the resulting voltage level at PAD is unpredictable, i.e., floating so that no valid logical expect value at the signal evaluation line 26 RDATA can be defined to be tested for.

1.3 OBJECTS OF THE INVENTION

It is thus the objective of the present invention to improve the testing of driver and that of receiver stages, and in particular that of combined stages, and in particular that of chip I/O stages.

2. SUMMARY AND ADVANTAGES OF THE INVENTION

These objects of the invention are achieved by the features stated in enclosed independent claims. Further advantageous arrangements and embodiments of the invention are set forth in the respective subclaims.

According to its broadest aspect the present invention provides a method for qualifying a leakage current to be tolerable or not, the leakage current being present in a test area of a hardware circuit, and in particular of a driver / receiver stage, or input/ output stage, respectively, which comprises said test area between a first tap node, and a second node being able to be forced to a voltage potential of a predefined value, for example ground, or supply voltage level Vdd, or any other predetermined voltage level. Said method comprises the steps of:
a) shutting off any operational current inflow into said test area,
b) generating an evaluabale voltage difference between said first

tap node and said second node, the voltage difference being characteristic for said leakage current,
c) qualifying said leakage current as tolerable in dependence of the resulting voltage at said first tap node.

The characteristic voltage difference can be a voltage drop in a test path comprising a specifically added switching element acting as an Ohm-resistor e.g., a transistor switched in pass mode having a predetermined operational resistivity and said test area connected in series to said resistor.

A key idea of the present invention is thus to provide an on-chip selftest feature, which provides valid voltage levels at the off-chip connection node PAD for a good device, which are convertable by the receiver to predictable logic states at the evaluation line RDATA. In case of a leakage or a HZ fail, the voltage level at PAD will not meet this requirement and will lead to a mismatch of the logical value, chip-internally expected at said signal line RDATA.

Advantageously, this can be done as follows:

Two dedicated support transistor devices are added into the prior art switching scheme, together with a simple control logic for selectively controlling them according to a predetermined test scheme to be performed autonomously on the chip without any test device external to the chip being required anymore. The test input is fed via input lines into said control logic and the test result can be read from a result signal line.

The first of the two support devices is denoted as 'support device Up' and abbreviated as SDU, whereas the second support device is denoted as 'support device down', further abbreviated as SDD. Both devices are transistors of small size, the resistivity parametrics of which are defined as a function of the maximum allowed leakage current further referred to as 'Ileak' (max) and as a function of the predetermined 'receiver rec'

voltage levels, further referred to herein as MPDL (Most Positive Down Level) and ' LPUL' (Least Positive Up Level, including a respective predetermined guardband thus yielding the V PAD voltages
VL = MPDL - guardband and
VH = LPUL + guardband.

In case of an intolerable leakage current on a path from eg. PAD to GND or PAD to VDD greater than Ileak max , or in case of a HZ-defect, causing either the N-device or the P-device not being completely shut off, the resulting voltage on V PAD will be greater than LPUL (receiver Least Positive Up Level) or smaller than MPDL (receiver Most Positive Down Level) such that the receiver will convert these failure-indicating voltage levels on the signal line RDATA to the opposite logical value of what is expected chip-internally and the test will fail.

The advantages are as follows:

An I/O Leakage Selftest is provided without the need of a tester connection to the pad node even in case of a reduced pin count test chip technology.

Further, this inventional principle automatically covers the high impedance (HZ) test of the signal I/O stage under test.

Further, the selftest can be achieved with a simple test scheme, applied just via the test input output signal lines.

Further, the test can be applied at low speed and thus there is no need for a prior art high performance test equipment.

Further, the test can be applied at every packing level: at wafer level, on a single-chip module (SCM) or on a temporary chip attach (TCA), on a multiple chip module (MCM), and even at system level, when the chip is incorporated into a printed circuit board connected to whatever bus system. In said latter

case, advantageously a dedicated piece of system software can be executed which controls the hardware logic according to the test scheme so as to performing the inventional test method. Said software might be run triggered by service staff, or, in any automated form.

Finally, a further improved, extended test scheme can be achieved by combining the tests described herein with the tests disclosed in the copending patent application with the title: „Selftest with splitted, asymmetric, controlled driver output stage". In combination, any further test device really becomes obsolete for said driver/receiver stages on a chip.

3. BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and is not limited by the shape of the figures of the accompanying drawings in which:

Fig. 1 is a simplified schematic logical representation of an exemplary implementation of a prior art bidirectional signal Input/Ouput stage,

Fig. 2 includes a schematic logical representation of an exemplary implementation of a combined Input/ Output stage with integrated leakage and Driver HZ selftest facility according to an inventional embodiment.

4. DESCRIPTION OF THE PREFERRED EMBODIMENT

With general reference to the figures and with special reference now to Fig. 2 the P-device transistor and the N-device transistor are depicted with reference sign 20 and 22, respectively, connected in series between supply voltage VDD and ground as it is the case with prior art depicted in fig. 1.

In order to be able to qualify the input/output stage to be

tolerable or not in terms of a leakage current to be too large or in terms of the existence of an erroneous driver-HZ state, the driver devices 20 and 22 must be shut-off such that no operational current flows between VDD and ground. In other words, when there is no operational current inflow into a test region schematically depicted in the drawing with a rectangle 44 two respective subportions, further referred to as two test areas 70,72 constituing said region 44 can be tested subsequently for the above mentioned purposes according a predetermined test scheme.

In order to do that the gate terminal of each transistor device 20 and 22, respectively is correspondingly controlled by a respective gate control signal. Both gate control signals are generated from input signals DDATA 46 and ACT 48, and corresponding AND-gates 50 and 52, respectively. The activation signal 48 is implemented to have the value '1' when a driver test shall be performed whereas the signal 46 DDATA reflects the two different operational driver states '0' and '1', respectively, but a value '0' at the activation signal 48 turns off (high impedance) both of the devices 20 and 22 to enable the leakage test mode.

In order to generate an evaluable voltage difference, i.e., a voltage drop between a fixed-potential node VDD, or ground, respectively, and a first tap node PAD 54, the voltage drop being considered to be characteristic for a leakage current to be tested for, a pair of high-resistive transistors 56 and 58, respectively denoted as a support device up (SDU), and support device down (SDD), are connected in series between the supply voltage VDD and ground in parallel to the two P-, N-devices 20 and 22, respectively. When said transistor devices 56 and 58 are controlled to be in a high-resistive pass mode a voltage drop can be generated by either of the two support devices. The gate terminal of devices 56 and 58 is controlled by a respective control signal generated by a respective AND-gate 60, and 62, respectively.

The input into these AND-gates is as follows:

A selftest signal 64 is fed into both of said AND-gates which when being '1' enables the selftest mode. When it is '0', instead, basically the regular operation of the I/O stage can be performed.

Further, the above mentioned activation signal 48 (ACT) is fed in an inverted form into the AND-gates 60, 62. The signal 46 (DDATA) is fed into AND-gate 60 and in an inverted form into AND-gate 62, so that, depending on the state of signal 46, the one or the other of the devices 56 and 58 are set into the high resistive pass mode.

The receiver 24 is connected to the tap node 54 (PAD) between the two support devices 56 and 58. The output RDATA 68 of said receiver 24 is written according to the voltage level applied at tap node 54 (PAD) and can be captured into a latch or fanned out to the test apparatus for further test result evaluation.

A preferred embodiment of the inventional selftest method will now be described in more detail with the switching scheme described above and with special respect to the receive hysteresis of the receiving device 24 which is depicted in the upper right corner of fig. 2, whereby a hysteresis must not necessarily been given, what means that MPDL can be equal to LPUL.

In short terms, each support device is controlled via an AND gate, connected to three different signal lines
ACT=driver inhibit,
DDATA=data signal,
SELFTEST.

The one or the other support device is switched ON if ACT=0,

SELFTEST=1 and specifically dependend on the state of DDATA with
DDATA=0 results in SDD=ON, and
DDATA=1 results in SDU=ON.

For any other signal combination the support devices are switched OFF.

In particular, when, initially, a value of '0' is applied at receiving device 24 a voltage larger than the least positive up-level (LPUL) must be applied at its input, for example at the tap node 54, to change its output RDATA 68 to a '1'. It should be noted that the tap node 54 is depicted in triple form but can be regarded as having the same voltage potential all the time.

Further, when a value of '1' was applied at the receiving device 24 a voltage smaller than the most positive down level (MPDL) must be applied at its input to change its output to a '0'.

For the test purposes of the present embodiment the signal RDATA is intended to reflect the test result. In particular, when an input/output stage is considered to be of intolerable quality the signal 68 RDATA is intended to be different from the signal DDATA. In case both signals, DDATA and RDATA have the same value, the input/output stage is considered to be of tolerable quality.

The following input pattern application sequence is now proposed to be applied as an input for the control signals selftest 64, DDATA 46 and ACT 48: First, DDATA is '1', selftest is '0' and ACT is '1'. With reference to the figure the respective table is given in an overview form, whereby an x-value for input means 'non-relevant, whereas for output 'undefined'. The before-mentioned value setting is depicted with the second column of said table.

In this situation the P-device 20 is switched into pass mode, the

N-device 22 is switched into lock mode, the support devices 56 and 58 are in lock mode as well. Thus, a resulting 'initial' voltage near to the supply voltage VDD can be measured at the tap node 54 leading to a value of '1' at the output of the receiver device 24 as RDATA signal 68.

Then, first the selftest signal 64 is switched from '0' to '1' and the ACT signal 48 is also switched, but from '1' to '0', third column. This means that the P-device 20, respectively, is shut-off now and with the signal DDATA having a value of '1' the AND-gate 62 is closed because the DDATA '1' is inverted before entered into the AND-gate 62.

As is described above the AND-gate 60 generates an output of '1' which is inverted after being output and applied to the gate input of the SDU-device 56. Thus, SDU-device 56 is switched into pass mode. As the output of AND-gate 62 is a '0' the support device 58 (SDD) is switched off which still keeps the node 54 at the initial state. Then, finally in the sequence, DDATA is switched from '1' to '0' so that SDU-device 56 is now switched off and SDD device 58 switched into pass mode.

Thus, a resulting test current flows from a test area of the test region 44, eg., the portion being schematically depicted in fig. 2 and having the reference sign 72, through the support device 58 to ground. Thus, the SDD-design and the test area 72 is connected in series and build up a characteristic voltage divider which is tapped on the tap node 54. When the leakage current is too large for the input/output stage to be qualified as tolerable a voltage drop to VDD would be generated from the leakage current which would prevent the receiver 24 in detecting a tolerable voltage of less or equal VL at the tap node 54.

According to the present invention the resistivity of the support device 58 and that of the support device 56 -which will be described later below- is dimensioned such that according to the quality requirements, i.e., the quality specifications of the

input/output stage, the voltage resulting from the test voltage drop is evaluated such that it defines the tolerable range when it is smaller than VL, see fig. 2 upright corner, which is a voltage level resulting from MPDL minus a certain, predetermined guardband. This reflects the need of the receiver hysteresis behavior having to be considered with the test result.

Thus, with the scheme described above the test area 72 representing some portion of the overall test region 44 is tested for I/O leakage current and erroneous driver-HZ which results to a leakage current, as well.

It should be noted that potential leakage defects at the receiver area 24, which should be part of the region 44 in fig.2, are covered too. Areas 70 and 72 should be understood herein as 'examples' for potential defect areas;

Then, for building up a similar test scheme for the remaining test area 70, see back to the switching scheme of fig. 2, but column 4 now, DDATA is kept at '0', ACT is switched to '1' and SELFTEST to '0' to apply the opposite initial state '0' on node 54 by having devices 20, 56 and 58 in lock mode and device 22 in pass mode, respectively, supposed in case the leakage current of test area 72 was tested small enough before, in order to satisfy the test quality requirements.

In the case ACT = '0', SELFTEST = '1' and later on in sequence DDATA = '1', see the most right column, the AND-gate 60 outputs a '0' after inversion and sets the support device 56 (SDU) in pass mode whereas device 22 gets into the lock mode. Support device 58, however, is set into lock mode because now the AND-gate 62 outputs a '0'. Thus, a test current now flows from VDD through the support device 56 into the test area 70.

The larger the leakage current through test area 70 the larger is now the voltage drop over support device 56 caused by said leakage current. Thus, when the leakage current is very small and

thus the device quality is gradually good, i.e. tolerable, a voltage would result on node 54 which is quite close to VDD. Accordingly, the leakage current can be qualified as being too high and thus the input/output stage could be qualified as being not tolerable when a voltage results at node 54 which is smaller then VH as it is depicted in fig. 2, top right corner.
VH in turn is defined as the voltage level LPUL plus the same guardband as described before. Thus, in case of intolerable quality due to a leakage current to be found to be too large a quite low voltage, i.e. less than VH would result at node 54 and would prevent the receiver device 24 output from a value of '0' to a value of '1'. Thus, in order to have correct test conditions, the receiver device 24 must output a '1' at RDATA 68.

In order to clarify the pattern application sequence and the resulting states at the node 54 and RDATA the following table is given in this text, again:

ACT	0	1	0	1	0
SELFTEST	0	0	1	0	1
DDATA	x	1	0	0	1
V PAD	float	~VDD	0V..VL	~0V	VH..VDD
RDATA	x	1	0	0	1

The upper portion of the table written above denotes the input section of the switching scheme depicted in fig. 2. The bottom portion comprising the voltage at node 54 PAD and the signal 68 RDATA describes the result section of the switching scheme. The first column describes an input state sequence which results in a floating voltage state to be retrievable on the node 54 PAD. In this situation no evaluable value can be found out in the evaluation signal RDATA.

Column 3 and column 5 represent the test situation, in which column 5 reflects the test of the occurrence of a leakage current

in the test area depicted with reference sign 70 in fig. 2. Column 3 reflects the test situation when test area 72 is tested.

Column 2 and column 4, respectively, reflect the regular operational mode of the switching scheme characterized by the selftest signal having the value of '0', as well as the initial states in the test application sequence whereby column 3 has to be applied after column 2 and column 5 after column 4.

In the foregoing specification the invention has been described with reference to a specific exemplary embodiment thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are accordingly to be regarded as illustrative rather than in a restrictive sense.

In particular, the control logic required for supplying the support devices 56 and 58 may be implemented differently corresponding to a specific situation being present on a respective chip.

The present invention can be realized in hardware, software, or a combination of hardware and software. A testing tool according to the present invention can be realized in a centralized fashion in one computer system, or in a distributed fashion where different elements are spread across several interconnected computer systems. Any kind of computer system or other apparatus adapted for carrying out the methods described herein is suited. A typical combination of hardware and software could be a general purpose computer system with a computer program that, when being loaded and executed, controls the computer system such that it carries out the methods described herein.

The present invention can also be embedded in a computer program product, which comprises all the features enabling the

implementation of the methods described herein, and which - when loaded in a computer system - is able to carry out these methods.

Computer program means or computer program in the present context mean any expression, in any language, code or notation, of a set of instructions intended to cause a system having an information processing capability to perform a particular function either directly or after either or both of the following

a) conversion to another language, code or notation;

b) reproduction in a different material form.

C L A I M S

1. A method for qualifying a leakage current to be tolerable or not, the leakage current being present in a test area (70,72) of a hardware circuit which comprises said test area between a first tap node (54) and a second node being able to be forced to a voltage potential of a predefined value,
comprising the steps of:
a) shutting off any operational current inflow into said test area,
b) generating an evaluabale voltage difference to said first tap node being characteristic for said leakage current, and
c) qualifying said leakage current as tolerable in dependence of the resulting voltage at said first tap node.

2. The method according to claim 1 in which said leakage current flows in a test path comprising a switching element (56,58) acting as an Ohm-resistor having a predetermined operational resistivity, and said test area (70, 72) being connected in series to said resistor.

3. The method according to the preceding claim in which said resistor (56,58) is a transistor switched in pass mode.

4. The method according to claim 1 in which said tap node (54) is a node between two transistors (56,58) SDU and SDD of a driver stage, building up a voltage divider with the test areas (70, 72).

5. The method according to the preceding claim in which a test region (44) comprising said test areas (70,72) includes a receiver device (24) of a combined driver/ receiver stage of a semiconductor chip.

6. The method according to the preceding claim used for qualifying and/ or quantifying the leakage current in a signal input/output book of a semiconductor chip.

7. A hardware circuit comprising
a leakage test area (70,72) between a first tap node (54) and a second node being arranged to be forcible to a voltage potential of a predefined value,
the circuit being characterized by:
a) means (46,48,50,52) for shutting off any operational current inflow into at least said leakage test area,
b) means (56,58) for generating an evaluable voltage difference between said first tap node and said second node being characteristic for said leakage current,
c) means (24) for qualifying and/or quantifying said leakage current as tolerable in dependence of the resulting voltage at said first tap node.

8. The hardware circuit according to the preceding claim in which said first node (54) is implemented as a tap node (54) of a voltage divider means (56,58).

9. The hardware circuit according to the preceding claim in which said voltage divider means is a pair of transistors (56,58) connected in series to test areas (70,72), and said tap node is connected between the drain of the first transistor (56) and the source of the second transistor (58) building up said pair,
the gate line of each of said transistors (56,58) being connected to selectively run two different test modes, in each of which a respective other transistor (56) is switched in pass mode and forms part of the test path when the respective other transistor (58) is switched in lock mode,

10. The hardware circuit according to the preceding claim being arranged as a combined input/output (I/O) stage of a semiconductor chip having a driving P device (20) comprising a plurality of P-type transistors and a driving N-device (22) comprising a second plurality of N-type transistors, said P-device and N-device being connected in series between two different voltage levels, said drive devices driving high, low, and HZ states to a terminal pad (54) connecting off from the

chip, the circuit further comprising
a receiving device (24) connected in parallel to said pad,
in which receiving device (24) the resistivity of one respective transistor (56,58) in pass mode is implemented as R-SDU = (VDD - VH) / Ileakmax with
VDD being the supply voltage,
VH being the voltage level associated with LPUL plus a guardband in the hysteresis of the receiving device (24), at which the receiving device is prevented from switching when coming from initial-state to the test-state of said I/O stage, and the resistivity of the other respective transistor (56,58) in pass mode is implemented as R-SDD = VL / Ileakmax with
VL being the voltage level associated with MPDL minus a guardband in the hysteresis of the receiving device (24), at which it is prevented from switching when coming from lower resistivity values associated with the pass mode of said I/O stage.

11. A single chip comprising the hardware circuit according to one of the preceding claims 7 to 10.

12. A single chip module comprising the hardware circuit according to one of the preceding claims 7 to 10.

13. A multi-chip module comprising the hardware circuit according to one of the preceding claims 7 to 10.

14. A printed circuit board comprising the hardware circuit according to one of the preceding claims 7 to 10.

15. A computer program for execution in a data processing system comprising computer program code portions for performing respective steps of the method according to anyone of the claims 1 to 6 when said computer program code portions are executed on a computer.

16. A computer program product stored on a computer usable medium comprising computer readable program means for causing a

computer to perform the method of anyone of the claims 1 to 6 when said computer program product is executed on a computer.

A B S T R A C T

The present invention relates to a test for leakage for driver/ receiver stages, and in particular for bi-directional input/ output stages (10) of a semiconductor chip.

Two dedicated support transistor devices (56,58) are added into the prior art switching scheme, together with a simple control logic (48,50,52,60,62,64) for selectively controlling them according to a predetermined test scheme.

By that an on-chip selftest feature provides valid voltage levels which are convertible by the receiver (24) to predictable logic states at the evaluation line RDATA. The test can be performed autonomously on the chip without any test device external to the chip being required anymore. (Fig.2)

(Drawings)

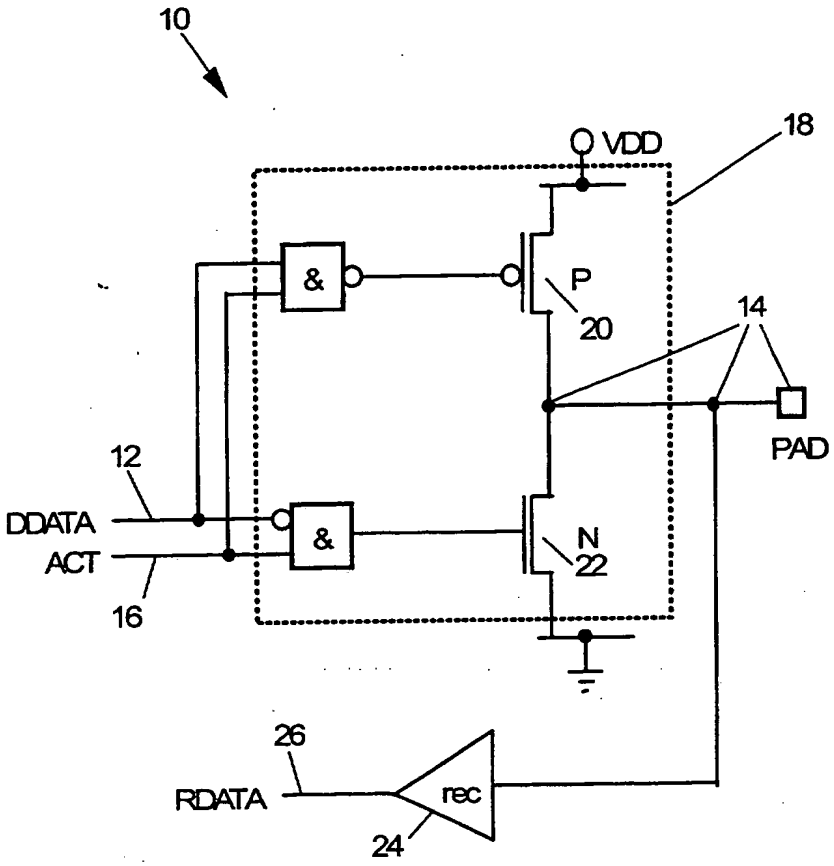
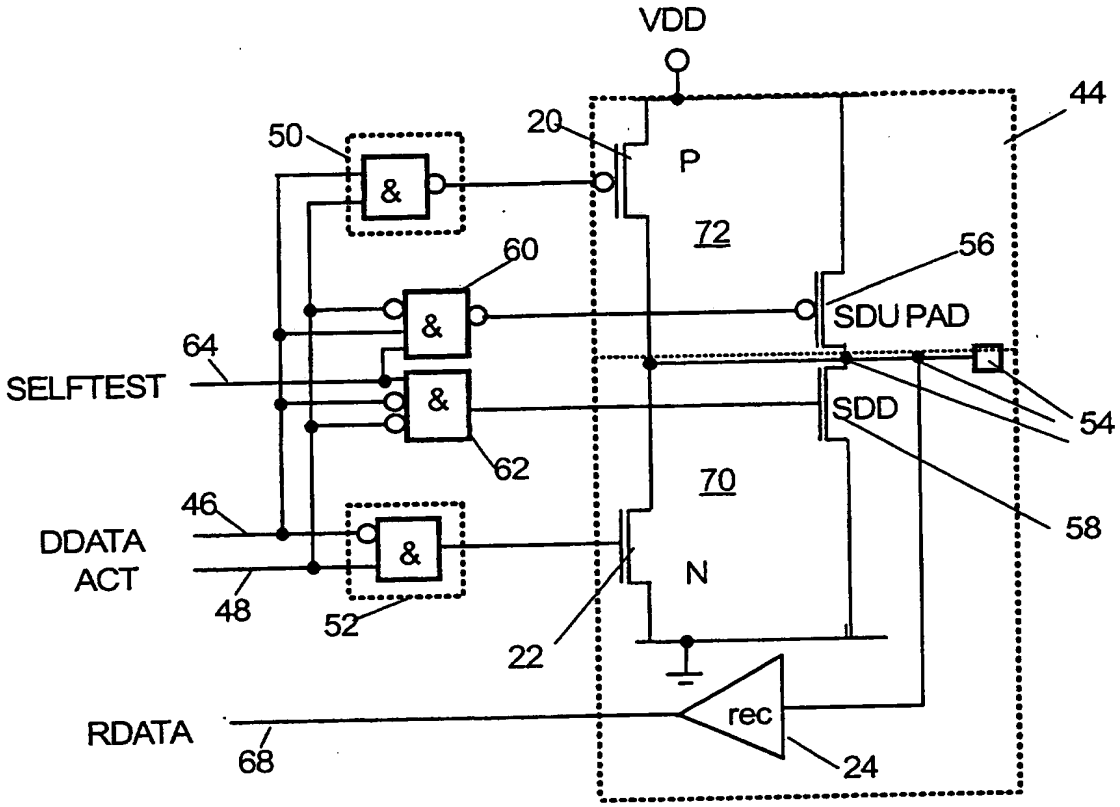
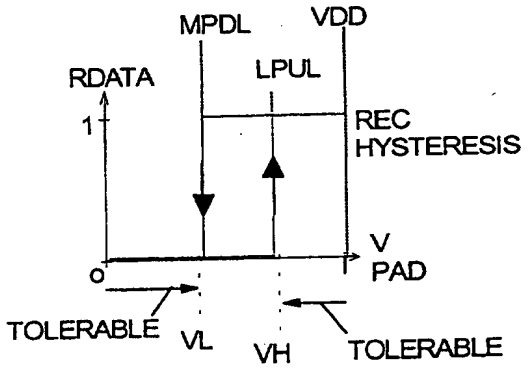


FIG. 1
PRIOR ART





ACT	0	1	0	1	0
SELFTEST	0	0	1	0	1
DDATA	X	1	0	0	1
V PAD	float	~VDD	0V..VL	~0V	VH..VDD
RDATA	X	1	0	0	1

FIG.2